

# Light-to-Light Readout System of the CMS Electromagnetic Calorimeter

P. Denes, J. M. Bussat, W. Lustermann, H. Mathez, P. Pangaud, and J. P. Walder

**Abstract**—For the Compact Muon Solenoid (CMS) experiment at the Large Hadron Collider (LHC) at CERN, an 80 000-crystal electromagnetic calorimeter will measure electron and photon energies with high precision over a dynamic range of roughly 16 bits. The readout electronics will be located directly behind the crystals, and must survive a total dose of up to  $2 \times 10^4 Gy$  along with  $5 \times 10^{13} n/cm^2$ . A readout chain consisting of a custom wide-range acquisition circuit, commercial ADC and custom optical link for each crystal is presently under construction. An overview of the design is presented, with emphasis on the large-scale fiber communication system.

## I. INTRODUCTION

THE Electromagnetic Calorimeter [1] of the Compact Muon Solenoid (CMS) experiment being constructed for the Large Hadron Collider (LHC) at CERN will consist of roughly 80 000 lead tungstate ( $PbWO_4$ ) crystals arranged in a barrel of 61 200 crystals and two endcaps of 7816 crystals each. The scintillation light from the crystals is captured by a photodetector (silicon avalanche photodiodes in the barrel and vacuum phototriodes in the endcaps), amplified, digitized and transported by high-speed fiber-optic links off the detector. The digitizing electronics on the detector must survive a total absorbed dose of up to  $2 \times 10^4 Gy$  along with a fluence of  $5 \times 10^{13} n/cm^2$  over the lifetime of the detector, which is defined to be the amount of time required to obtain an integrated luminosity of  $5 \times 10^5 pb^{-1}$ . The endcap photodetectors must operate up to  $10^{14} n/cm^2$ , however, the digitizing electronics will be placed in such a way as to limit the total fluence to  $5 \times 10^{13} n/cm^2$ .

Following the digitizing electronics, digital signal processing circuitry pipelines the data and performs a variety of numerical calculations for use in the experiment trigger. In order to avoid placing this large quantity of digital electronics in the detector radiation environment, fiber-optic links, one per crystal, will be used to transport the digitized data off the detector into a shielded environment. Thus, the on-detector readout starts with an optical to electrical conversion, and ends with an electrical to optical conversion.

Manuscript received November 3, 2000; revised February 3, 2001. This work was supported in part by the U.S. Department of Energy under Grant DE-FG02-91ER40671.

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Publisher Item Identifier S 0018-9499(01)05075-4.

## II. SYSTEM REQUIREMENTS

The Electromagnetic Calorimeter is composed of  $PbWO_4$  crystals located in the 4 T CMS magnetic field.  $PbWO_4$  has a principal decay time of  $\sim 10$  ns, and a light yield in full-size crystals of  $< 100$  photons/MeV. The most challenging physics signal for the detector is  $H \rightarrow \gamma\gamma$ , with photons in the range of 20 to 100 GeV, where sub-percent resolution is required. In the region up to around 300 GeV, good resolution is still required in order to reconstruct  $Z \rightarrow e^+e^-$  and reject backgrounds. At very high energies, resolution should be sufficient to reconstruct  $Z' \rightarrow e^+e^-$ .

### A. Photodetectors

The low light yield and high collision frequency (40 MHz) combined with the need for excellent resolution at energies  $< 100$  GeV requires a photodetector with gain. The strong perpendicular magnetic field in the barrel precludes the use of vacuum detectors, whereas the high radiation levels in the very forward direction of the endcaps argue against solid state photodetectors. As a result, the ECAL will use large-area silicon avalanche photodiodes (APD) in the barrel [2] and vacuum phototriodes (VPT) in the endcaps [3]. Two APDs of  $5 mm \times 5 mm$  area each are used per crystal, operating at a gain of 50. In the endcaps, the phototriode has a 22 mm diameter active area, and a gain of at least 6 (in the magnetic field). The APDs, along with their wiring, present 200 pF at the input of the preamplifier, and the VPT's present 40 pF. At the barrel-endcap division, the photodetectors have a  $26^\circ$  angle with respect to the magnetic field.

Fig. 1 shows the anticipated energy resolution for the sum of several crystals in the barrel. The resolution has been parameterized as

$$\frac{\sigma}{E} = \frac{A}{\sqrt{E}} \oplus c \oplus \sqrt{\frac{F}{N_{pe}E}} \oplus \frac{b}{E} \quad (1)$$

where

$E$	energy in GeV;
$A$ ( $\sim 2\%$ )	given by shower containment;
$c$ ( $\sim 0.55\%$ )	constant term which includes calibration error;
$F$	excess noise factor;
$N_{pe}$	number of photoelectrons/MeV;
$b$	electronics noise in the crystal sum.

Taking into account the spread of crystal light yields and photodetector gains, the full-scale energy is set at 1.5 TeV in the barrel and is 3.0 TeV in the endcaps, with a dynamic range

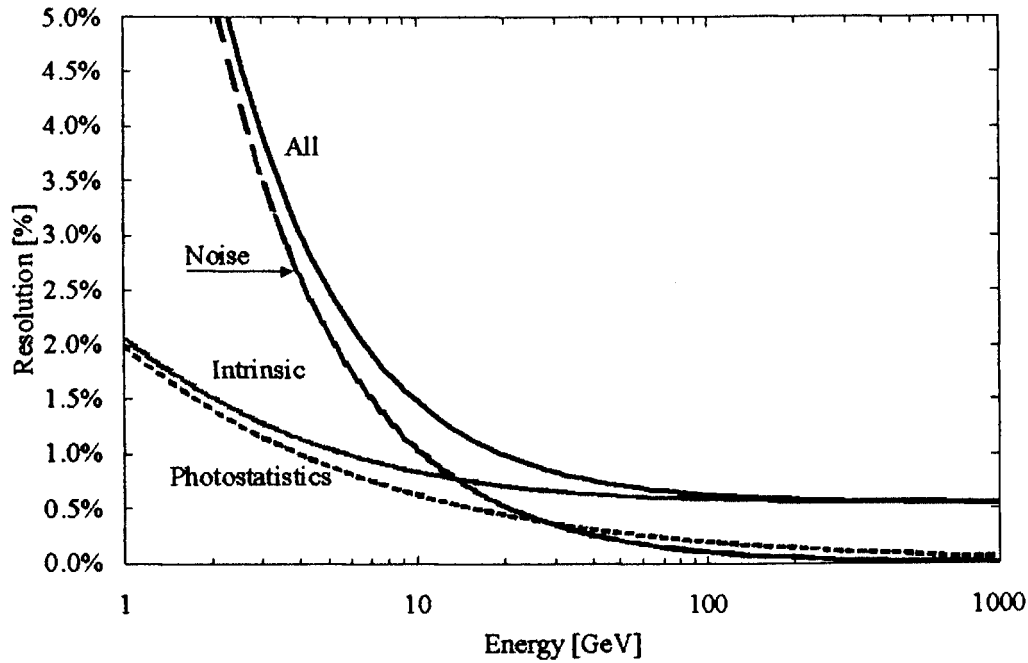


Fig. 1. Energy resolution in the ECAL barrel at low luminosity. The four curves represent the intrinsic crystal resolution, the photostatistics contribution, the noise at low luminosity and all effects taken together.

requirement of 15.2 bits. In order to minimize complexity in the front-end circuit, energy, rather than transverse energy, is readout.

### B. Readout Topology

The readout design is driven by the technical requirements to capture the signal (dynamic range, linearity better than the constant term, noise, etc.), the digital trigger of CMS and the limited space available for electronics and cables. In order to construct the highest quality trigger primitives, data from individual crystals are processed and then summed. This implies a 40 MHz digitizing element per crystal.

The physical readout geometry is fixed by the calorimeter. Readout units service 10 crystals. In the barrel, 25 crystals form a trigger tower and in the endcaps, crystals are mapped from an  $r\phi$  geometry into towers. A 10-crystal unit is serviced by one 12-fiber ribbon: 10 fibers transport data off the detector at high speed, and the two remaining fibers are used to bring the LHC bunch crossing clock and a slow serial interface to the detector. Off-detector, 100-channel units pipeline the data from ten readout units, form trigger primitives and transmit accept events to the data acquisition system.

## III. ELEMENTS OF THE READOUT

### A. Front-End Circuit

The signal capture electronics consists of a custom monolithic floating-point preamplifier [4], [5] (FPPA) which contains a wide dynamic range preamplifier, sample/hold and gain-multiplexing circuits. The FPPA is followed by a 40 MHz 12-bit ADC (Analog Devices AD9042). Both the FPPA and ADC [6] are fabricated in dielectrically isolated, full complementary bipolar processes.

The preamplifier converts the photocurrent into a voltage with a dynamic range of around 15 bits. This voltage is then amplified by four clamping amplifiers with gains of 1, 5, 9, or 33. The gain-multiplexing circuit simultaneously samples each of these four voltages at the LHC bunch crossing frequency of 40 MHz. Voltage comparators and digital logic in the circuit then determine which of the four voltage samples is the largest (corresponding to the highest gain) below a certain saturation threshold. This (quasistatic) voltage is multiplexed and digitized by the ADC. The output data consist of a floating-point representation of the data in the form

$$G_2 G_1 G_0 D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0$$

where

- $G_2$  data type flag;
- $[G_1, G_0]$  2-bit code representing the gain range used (1, 5, 9, 33);
- $[D_{11} \dots D_0]$  12-bit ADC mantissa.

In this way, the 12-bit ADC converts the full 16-bit dynamic range, and the ADC quantization error is always small with respect to the detector energy resolution.

The FPPA is a voltage sampling circuit, which allows the performance to be modified as a function of luminosity. The noise curve shown in Fig. 1 is the noise at low luminosity. At low luminosity, the best performance is obtained by adding several samples to determine the signal height, and then subtracting the average of several samples well before the peak as pedestal estimators. As the luminosity increases, pileup noise can dominate, and the best overall resolution is obtained with the peak sample, subtracting the closest baseline pre-sample. For the waveform shown in Fig. 2, this corresponds to the difference between the points labeled "Pk" and "Pk-3."

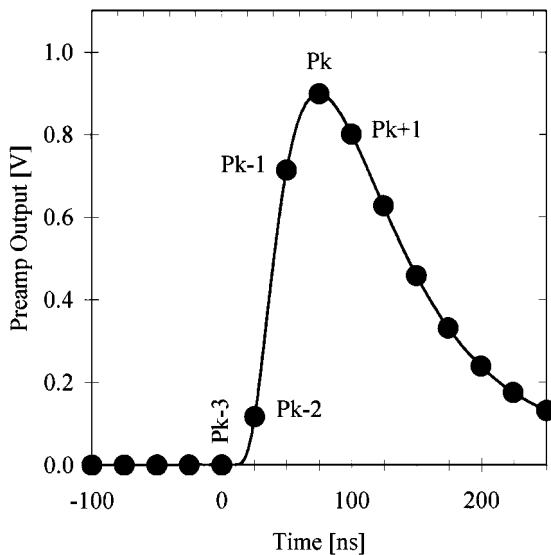


Fig. 2. Example of voltage-sampled waveform. The curve represents the preamplifier output, and the solid circles represent the sampled values.

As the luminosity increases, an additional reason to limit the number of samples used is the increased leakage current in the APDs. Displacement damage in APDs results in increased leakage current. The portion of leakage current which arises in the bulk undergoes amplification, which is a correlated process, and in addition has non-Poisson statistics, as represented by the excess noise factor.

1) *Slow Control*: The frontend circuitry is also used to monitor the detector environmental status. The FPPA output multiplexer consists of eight switches, four of which are used for the signal ( $G_2 = 0$ ) and four more ( $G_2 = 1$ ) which are used to condition an external temperature sensor, measure the APD leakage current and check the internal functions of the FPPA.

### B. Fiber-Optic Transmitter

The fiber readout system consists of several elements: the high-speed transmitters and receivers which send data for each crystal off the detector, the lower-speed transmitters and receivers which send the clock and configuration data to the detector, the electro-optic elements, the connectors and the fiber itself.

The high-speed transmitter and clock receiver are custom developments due to the radiation environment in the ECAL. In addition, the large number of channels requires a low power design ( $<300$  mW per transmitter). The remaining components are commercial. To minimize cost, standard  $62.5 \mu/125 \mu$  multi-mode fibers with 850 nm VCSELs are used (as there are several fibers available which do not suffer extensive radiation damage in our environment).

The high-speed receiver, being off-detector, can be a commercial part, so the line encoding protocol should correspond to a commercial standard. Two widely used protocols were considered, IBM's 8B/10B encoding [7], used in Gigabit Ethernet and Agilent's CIMT (Conditional Invert, Master Transition) [8] used in the G-Link. CIMT is a length-independent frame-oriented protocol, whereas 8B/10B is packet oriented. Although both protocols are similar, CIMT is simpler to implement and

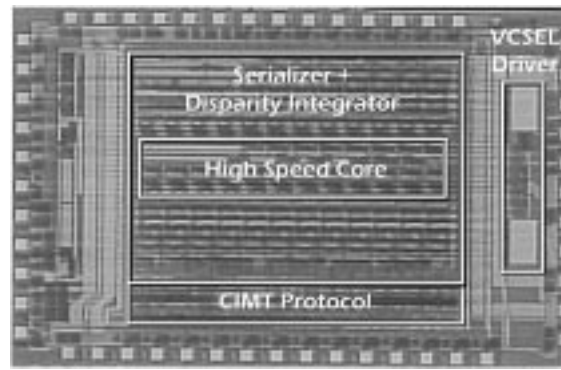


Fig. 3. CHFET fiber-optic transmitter. The circuit, which measures  $4 \text{ mm} \times 3 \text{ mm}$  contains encoding protocol, serializer and VCSEL driver.

is better suited to the synchronous, continuous environment as synchronization loss is more rapidly and reliably detected. (Synchronization loss, which results in dead time and data loss is a more serious problem in the ECAL readout than random bit errors.) In both cases, 20 bits are required to transmit a 16-bit word.

A fiber-optic transmitter meeting the radiation and power requirements has been constructed in CHFET (Complementary Heterostructure FET) GaAs technology [9]. The design aims for a single-chip solution, with serializer, protocol encoder and VCSEL driver on the same chip.

A first proof-of-principle version [10] was submitted in November 1997. This circuit consisted of a 20-bit serializer, converting 20 parallel inputs with a 40 MHz word rate into an 800 MB/s optical output stream. The circuit consumed considerably less power than the maximum allowed (90 mW including VCSEL at 800 MB/s) but suffered from extreme electrostatic discharge (ESD) sensitivity and asymmetry in the VCSEL output.

An improved version, which included 16-bit G-Link protocol was submitted in February 1999. The circuit, shown in Fig. 3, contains 6108 transistors and is  $12 \text{ mm}^2$ .

In addition to the choice of encoding protocol, an additional design consideration was the clocking scheme used to accomplish serialization. Conventional serializers employ phase-locked loops (PLLs) to multiply the word clock (40 MHz in this case) up to the serial bit rate (800 MB/s in this case). The serializer then consists of a multiplexer/flip-flop chain running at the bit rate.

A PLL-based approach has two potential drawbacks in the ECAL: a potentially higher rate of synchronization loss due to single-event effects in the PLL and potentially higher power consumption due to the high-speed flip-flops. For those reasons, this design uses a delay-locked loop (DLL) rather than a PLL. A PLL consists of a voltage controlled oscillator, divider and phase/frequency detector. The DLL consists of voltage controlled delay elements and a phase detector.

1) *Delay-Locked Loop*: The voltage controlled delay element is shown in Fig. 4. A cross-coupled configuration was chosen in order to use differential clocks throughout, but avoid the standing current required for the conventional differential pair-based delay cell. This version is slightly modified with respect to the previous chip. The original version consisted

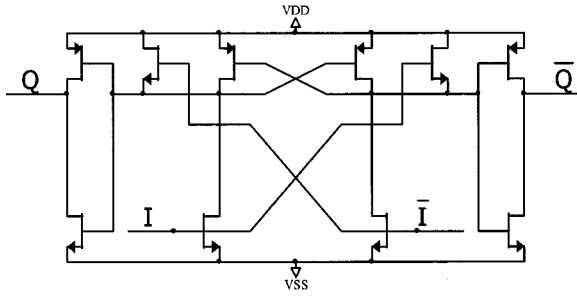


Fig. 4. Voltage controlled delay element used in the DLL.

of simply the cross-coupled inverters, whereas here an output buffer with  $N$ -channel follower was added. The additional stages actually increase the speed (a key design constraint in CHFET is that  $\beta_N/\beta_P \geq 10$ ). This cell has a nominal delay of  $\Delta t = 400$  ps at 1.3 V (typical CHFET logic operating voltage) with a slope of  $d\Delta t/dV_{DD} = -600$  ps/V. Three such elements are used per bit.

A phase comparator consisting of cross-clocked flip-flops (the clock exiting the DLL clocks a flip-flop whose data is the input clock and vice versa) drives a charge pump which sets the DLL control voltage. Such a simple phase detector cannot work for a PLL, which requires some degeneracy to lock, however the DLL is a first order capture problem so this scheme works well. The phase advance is set by an external integrating capacitor. With the 100  $\mu$ A bias current in the charge pump, a capacitor of at least 5 nF ensures a phase advance less than 25 ps/25 ns clock. Further, as the DLL has no “memory,” unlike the PLL, a single-event effect in the DLL cannot change the phase by more than 25 ps/25 ns clock.

2) *Combinatorial Logic:* The combinatorial logic used to create the high-speed bit stream must support very fast edge rates, and was thus constructed using  $N$ -channel devices only, in a fashion reminiscent of NMOS logic. The combinatorial cell for each bit is shown in Fig. 5. The  $Q$  outputs of for each of the bits are then combined by an OR tree, made in the same  $N$ -channel logic.

The basic combinatorial function for the  $i$ th bit is to take the overlap of the data bit ( $D_i$ ), the DLL tap corresponding to  $i$ th delayed clock ( $K_i$ ) and the inverse of the  $i + 1$ st delayed clock

$$Q_i = D_i \cdot K_i \cdot \overline{K_{i+1}}. \quad (2)$$

This logic is susceptible to glitches between bit transitions, so the cell in Fig. 5 has a look-ahead function added

$$Q_i = D_i \cdot K_i \cdot \overline{K_{i+2}} \cdot [D_{i+1} \cdot K_{i+1}] \cdot [\overline{D_{i+1}} \cdot \overline{K_{i+2}}]. \quad (3)$$

Each combinatorial cell requires roughly 1 mA and has an output swing of typically 0.7 V. As the cell is essentially a switched current source, the output swing is always correctly adapted for the input, even over a wide range of process variation.

3) *Output Stage:* The complete circuit operates from a single 2-V power supply. An internal regulator generates the 1.3 V needed for the CMOS-like 40 MHz logic (input registers and all logic needed to implement the CIMT protocol), while

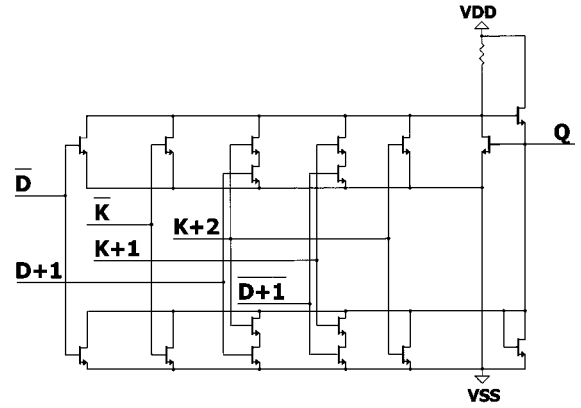


Fig. 5. Combinatorial logic cell used to serialize one bit.  $D$  and  $K$  are the data and delayed clock corresponding to bit  $i$ .  $D + 1$  and  $K + 1$  correspond to bit  $i + 1$ , etc.

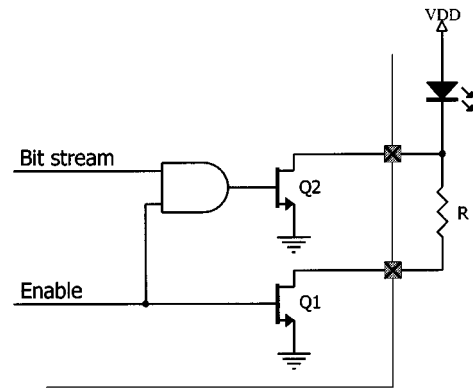


Fig. 6. VCSEL driver with open fiber control enable.

the high speed combinatorial logic operates directly from the 2 V supply.

The high output conductance of the GaAs transistors makes possible a VCSEL driver with  $< 200$  mV across the output transistor Q2 (the 2 V chip supply—the 1.8 V forward VCSEL voltage). An Open Fiber Control circuit asserts the Enable signal if the clock is present. When Enable is active, Q1 acts as a low resistance switch to generate bias current  $(V_{DD} - V_F)/R$  in the VCSEL, where  $V_F$  is the VCSEL forward voltage, and Q2 is used to modulate the VCSEL. If the clock is absent for more than 200 ns, Enable is deasserted and both the modulation and bias transistors switch off.

The complete circuit operating at 800 MB/s dissipates  $\sim 120$  mW. The bias resistor ( $R$  in Fig. 6) is set to 40  $\Omega$  to give 5 mA of VCSEL bias. The output transistors are sized to provide roughly 10 mA of modulation current, which results in  $\geq 500$   $\mu$ W of optical power launched into a 62.5  $\mu$ m/125  $\mu$ m fiber.

### C. Clock and Control Circuit

The 40 MHz LHC clock and some configuration data must be transported to each 10-channel readout unit. Low jitter clock recovery is essential for proper operation of the serializers, and excellent single-event immunity is required for the configuration registers. The readout configuration consists of programming the operating mode of the FPPAs and asserting or de-asserting the line that forces the serializers to send synchronization

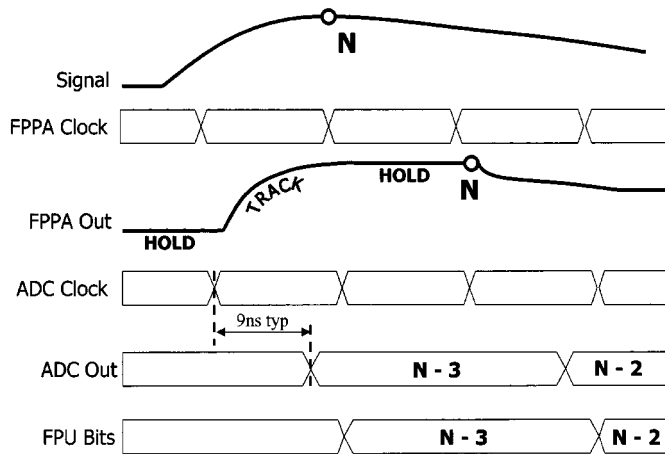


Fig. 7. Timing diagram.

frames. The FPPAs and serializers are identically programmed in parallel. By design, the command inputs are not latched, thus the control circuit configuration registers are the only configuration storage elements in the readout.

A circuit accomplishing these tasks has been fabricated in DMILL BiCMOS SoI technology. The 10 mm<sup>2</sup> chip has two p-i-n diode inputs, one carrying the clock and the other carrying a serial data stream. The serial stream utilizes a trivial self-latching protocol: 16-bit data along with a header are clocked through an input shift register. Once the header is detected the data are transferred to the configuration register and the shift register is cleared.

The clock receiver drives differential PECL output stages which are used to distribute the clock throughout the readout unit. One clock goes to the FPPAs in parallel, and one to the serializers. In order to save power, each FPPA generates the encode clock for its ADC. The recovered clock has a jitter of 20 ps with no non-Gaussian tails when the pin diode is driven by a VCSEL with 5 mA bias, 10 mA modulation using 62.5  $\mu$ m/125  $\mu$ m fiber.

The overall timing diagram is shown in Fig. 7. The received clock controls the FPPA Sample/Hold, and thus determines the event timing. The ADC clock is generated by the FPPA such that the ADC encodes the FPPA output at the end of the hold phase. The ADC has an internal latency of 3 clock cycles in total, so that when event  $N$  is being sampled, event  $N-3$  presents at the ADC output. The FPPA includes delay flip-flops that synchronize the gain code (labeled FPU Bits in Fig. 7) with the ADC output. The serializer includes one pipeline delay, during which it calculates the disparity and inverts the data if necessary. The first serialized

bit appears at the negative edge of the clock, so that the total latency in the on-detector readout is 5.5 clock cycles.

#### IV. INTERFACES

Optical signals will be transported between the detector and the counting room on 5  $\times$  12 fiber loose-tube cables. Each group of 12 fibers is terminated in a parallel connector, and the parallel connectors plug into a custom 5-connector adapter. To connect to the readout, a harness with one parallel connector and 12 individual connectors is used. The individual connectors go to surface-mount VCSELs, p-i-n diodes or high-speed receivers (in the counting room). The fiber connectivity has been developed in such a way that it can be used both on and off the detector.

Low- and high-voltage power are brought to the detector by groups of 50 crystals. Linear supplies [11] are used, with an intentionally low channel count in order to minimize any effects from supply failures. A suitably radiation-hard dc power regulator for use in the detector has been built and tested.

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